STATUS REGISTER

The Status Register indicates the state of interrupt conditions and other non-interrupt status lines. The interrupt conditions are the Data Set Ready, Data Carrier Detect, Transmitter Data Register Empty and Receiver Data Register Full as reported in bits 6 through 3, respectively. If any of these bits are set, the Interrupt (IRQ) indicator (bit 7) is also set. Overrun, Framing Error, and Parity Error are also reported (bits 2 through 0 respectively).

7	6	5	4	3	2	1	0
IRQ	$\overline{DSR}$	$\overline{DCD}$	TDRE	RDRF	OVRN	FE	PE

Bit 7 Interrupt (IRQ)
- 0 No interrupt
- 1 Interrupt has occurred

Bit 6 Data Set Ready ($\overline{DSR}$)
- 0 $\overline{DSR}$ low (ready)
- 1 $\overline{DSR}$ high (not ready)

Bit 5 Data Carrier Detect ($\overline{DCD}$)
- 0 $\overline{DCD}$ low (detected)
- 1 $\overline{DCD}$ high (not detected)

Bit 4 Transmitter Data Register Empty
- 0 Not empty
- 1 Empty

Bit 3 Receiver Data Register Full
- 0 Not full
- 1 Full

Bit 2 Overrun*
- 0 No overrun
- 1 Overrun has occurred

Bit 1 Framing Error*
- 0 No framing error
- 1 Framing error detected

Bit 0 Parity Error*
- 0 No parity error
- 1 Parity error detected

*No interrupt occurs for these conditions

Reset Initialization

7	6	5	4	3	2	1	0	
0	—	—	1	0	0	0	0	**Hardware reset**
—	—	—	—	—	0	—	—	**Program reset**

Parity Error (Bit 0), Framing Error (Bit 1), and Overrun (2)

None of these bits causes a processor interrupt to occur, but they are normally checked at the time the Receiver Data Register is read so that the validity of the data can be verified. These bits are self clearing (i.e., they are automatically cleared after ~~a read of the Receiver Data Register).~~ receive of a new character-

Receiver Data Register Full (Bit 3)

This bit goes to a 1 when the ACIA transfers data from the Receiver Shift Register to the Receiver Data Register, and goes to a 0 (is cleared) when the processor reads the Receiver Data Register.

Transmitter Data Register Empty (Bit 4)

This bit goes to a 1 when the ACIA transfers data from the Transmitter Data Register to the Transmitter Shift Register, and goes to a 0 (is cleared) when the processor writes new data onto the Transmitter Data Register.

Data Carrier Detect (Bit 5) and Data Set Ready (Bit 6)

These bits reflect the levels of the $\overline{DCD}$ and $\overline{DSR}$ inputs to the ACIA. A 0 indicates a low level (true condition) and a 1 indicates a high level (false). Whenever either of these inputs change state, an immediate processor interrupt (IRQ) occurs, unless bit 1 of the Command Register (IRD) is set to a 1 to disable IRQ. When the interrupt occurs, the status bits indicate the levels of the inputs immediately after the change of state occurred. Subsequent level changes will not affect the status bits until the Status Register is interrogated by the processor. At that time, another interrupt will immediately occur and the status bits reflect the new input levels. These bits are not automatically cleared (or reset) by an internal operation.

Interrupt (Bit 7)

This bit goes to a 1 whenever an interrupt condition occurs and goes to a 0 (is cleared) when the Status Register is read.

CONTROL REGISTER

The Control Register selects the desired ... source, word length, and the number of ...

7	6	5	4	3	2
SBN	WL		RCS	SB	
	WL1	WL0		SBR3	SBR2

Bit 7 Stop Bit Number (SBN)
- 0 1 Stop bit
- 1 2 Stop bits
- 1 1½ Stop bits For WL = 5 and no parity
- 1 1 Stop bit For WL = 8 and parity

Bits 6-5 Word Length (WL)

6	5	No. Bits
0	0	8
0	1	7
1	0	6
1	1	5

Bit 4 Receiver Clock Source (R
- 0 External receiver clock
- 1 Baud rate

Bits 3-0 Selected Baud Rate (SBR

3	2	1	0	Baud
0	0	0	0	16x External C
0	0	0	1	50
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	**Hardware rese**
—	—	—	—	—	—	—	—	**Program rese**

CONTROL REGISTER

The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.

7	6	5	4	3	2	1	0
SBN	WL		RCS	SBR			
	WL1	WL0		SBR3	SBR2	SBR1	SBR0

Bit 7 Stop Bit Number (SBN)

Bit 7	Stop Bit Number (SBN)
0	1 Stop bit
1	2 Stop bits
1	1½ Stop bits For WL = 5 and no parity
1	1 Stop bit For WL = 8 and parity

Bits 6-5 Word Length (WL)

6	5	No. Bits
0	0	8
0	1	7
1	0	6
1	1	5

Bit 4 Receiver Clock Source (RCS)

Bit 4	Receiver Clock Source (RCS)
0	External receiver clock
1	Baud rate

Bits 3-0 Selected Baud Rate (SBR)

3	2	1	0	Baud
0	0	0	0	16x External Clock
0	0	0	1	50
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	**Hardware reset ($\overline{RES}$)**
-	-	-	-	-	-	-	-	**Program reset**

Selected Baud Rate (Bits 0, 1, 2, 3)

These bits select the Transmitter baud rate, which can be at $^1/_{16}$ an external clock rate or one of 15 other rates controlled by the internal baud rate generator.

If the Receiver clock uses the same baud rate as the transmitter, then RxC becomes an output and can be used to slave other circuits to the ACIA. Figure 3 shows the Transmitter and Receiver layout.

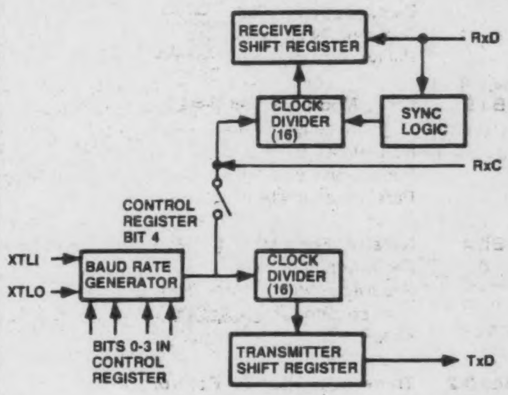

Figure 3. Transmitter/Receiver Clock Circuits

Receiver Clock Source (Bit 4)

This bit controls the clock source to the Receiver. A 0 causes the Receiver to operate at a baud rate of $^1/_{16}$ an external clock. A 1 causes the Receiver to operate at the same baud rate as is selected for the transmitter.

Word Length (Bits 5, 6)

These bits determine the word length to be used (5, 6, 7 or 8 bits).

Stop Bit Number (Bit 7)

This bit determines the number of stop bits used. A 0 always indicates one stop bit. A 1 indicates 1½ stop bits if the word length is 5 with no parity selected, 1 stop bit if the word length is 8 with parity selected, or 2 stop bits in all other configurations.

COMMAND REGISTER

The Command Register controls specific modes and functions.

7	6	5	4	3	2	1	0
PMC		PME	REM	TIC		IRD	DTR
PMC1	PMC0			TIC1	TIC0		

Bits 7-6 Parity Mode Control (PMC)

7	6	
0	0	Odd parity transmitted/received
0	1	Even parity transmitted/received
1	0	Mark parity bit transmitted Parity check disabled
1	1	Space parity bit transmitted Parity check disabled

Bit 5 Parity Mode Enabled (PME)

0	Parity mode disabled No parity bit generated Parity check disabled
1	Parity mode enabled

Bit 4 Receiver Echo Mode (REM)

0	Receiver normal mode
1	Receiver echo mode bits 2 and 3 Must be zero for receiver echo mode, RTS will be low.

Bits 3-2 Transmitter Interrupt Control (TIC)

transmitter

3	2	
0	0	$\overline{RTS}$ = High, transmit interrupt disabled
0	1	$\overline{RTS}$ = Low, transmit interrupt enabled
1	0	$\overline{RTS}$ = Low, transmit interrupt disabled
1	1	$\overline{RTS}$ = Low, transmit interrupt disabled transmit break on TxD

Bit 1 Interrupt Request Disabled (IRD)

0	$\overline{IRQ}$ enabled
1	$\overline{IRQ}$ disabled

Bit 0 Data Terminal Ready (DTR)

0	Data terminal not ready ($\overline{DTR}$ high)
1	Data terminal ready ($\overline{DTR}$ low)

Reset Initialization

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	**Hardware reset ($\overline{RES}$)**
—	—	—	0	0	0	0	0	**Program reset**

$\overline{RTS}$ IE En

00
01
10
11

Data Terminal Ready (Bit 0)

This bit enables all selected interrupts and controls the state of the Data Terminal Ready ($\overline{DTR}$) line. A 0 indicates the microcomputer system is not ready by setting the $\overline{DTR}$ line high. A 1 indicates the microcomputer system is ready by setting the $\overline{DTR}$ line low.

Receiver Interrupt Control (Bit 1)

9

This bit disables the Receiver from generating an interrupt when set to a 1. The Receiver interrupt is enabled when this bit is set to a 0 and Bit 0 is set to a 1.

Transmitter Interrupt Control (Bits 2, 3)

These bits control the state of the Ready to Send ($\overline{RTS}$) line and the Transmitter interrupt.

Receiver Echo Mode (Bit 4)

A 1 enables the Receiver Echo Mode and a 0 enables the Receiver Echo Mode. When bit 4 is a 1, bits 2 and 3 must be 0. In the Receiver Echo Mode, the Transmitter returns each transmission received by the Receiver delayed by one-half bit time.

Parity Mode Enable (Bit 5)

This bit enables parity bit generation and checking. A 0 disables parity bit generation by the Transmitter and parity bit checking by the Receiver. A 1 bit enables generation and checking of parity bits.

Parity Mode Control (Bits 6, 7)

These bits determine the type of parity generated by the Transmitter, (even, odd, mark or space) and the type of parity check done by the Receiver (even, odd, or no check).

INTERFACE SIGN

Figure 4 shows the ACIA
microprocessor and the r

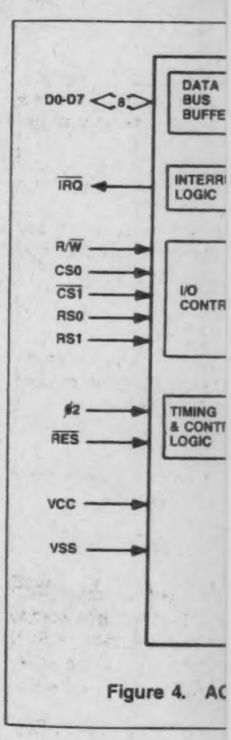

Figure 4. AC

MICROPROCESSOR IN

Reset ($\overline{RES}$)

During system initialization
hardware reset to occur. U
and the Control Register
Status Register is cleared
of Data Set Ready and Data
controlled by the $\overline{DSR}$ and
bit, which is set. $\overline{RES}$ must
for a reset to occur.

Input Clock (Ø2)

The input clock is the system
fers between the system m

Read/Write (R/$\overline{W}$)

The R/$\overline{W}$ input, generated
direction of data transfers.
processor to read the data
a write to the ACIA.

INTERFACE SIGNALS

Figure 4 shows the ACIA interface signals associated with the microprocessor and the modem.

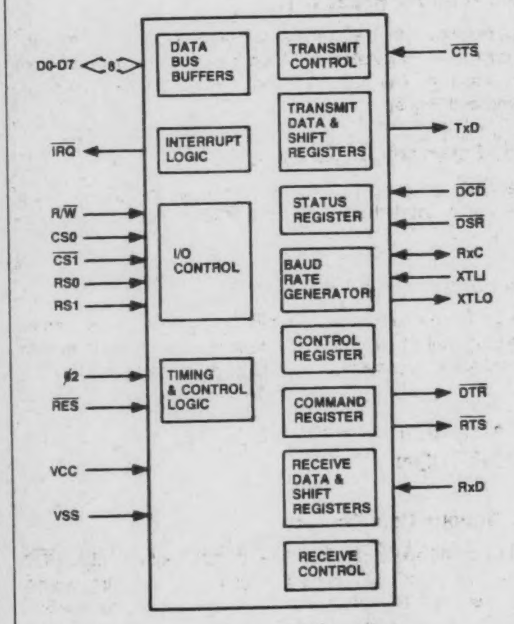

Figure 4. ACIA Interface Diagram

MICROPROCESSOR INTERFACE

Reset (RES)

During system initialization a low on the RES input causes a hardware reset to occur. Upon reset, the Command Register and the Control Register are cleared (all bits set to 0). The Status Register is cleared with the exception of the indications of Data Set Ready and Data Carrier Detect, which are externally controlled by the DSR and DCD lines, and the transmitter Empty bit, which is set. RES must be held low for one Ø2 clock cycle for a reset to occur.

Input Clock (Ø2)

The input clock is the system Ø2 clock and clocks all data transfers between the system microprocessor and the ACIA.

Read/Write (R/W)

The R/W input, generated by the microprocessor controls the direction of data transfers. A high on the R/W pin allows the processor to read the data supplied by the ACIA, a low allows a write to the ACIA.

Interrupt Request (IRQ)

The IRQ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common IRQ microprocessor input. Normally a high level, IRQ goes low when an interrupt occurs.

Data Bus (D0-D7)

The eight data line (D0-D7) pins transfer data between the processor and the ACIA. These lines are bi-directional and are normally high-impedance except during Read cycles when the ACIA is selected.

Chip Selects (CS0, CS1)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The ACIA is selected when CS0 is high and CS1 is low. When the ACIA is selected, the internal registers are addressed in accordance with the register select lines (RS0, RS1).

Register Selects (RS0, RS1)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various ACIA internal registers. Table 1 shows the internal register select coding.

Table 1. ACIA Register Selection

RS1	RS0	Register Operation: R/W = Low	Register Operation: R/W = High
L	L	Write Transmit Data Register	Read Receiver Data Register
L	H	Programmed Reset (Data is "Don't Care")	Read Status Register
H	L	Write Command Register	Read Command Register
H	H	Write Control Register	Read Control Register

Only the Command and Control registers can both be read and written. The programmed Reset operation does not cause any data transfer, but is used to clear bits 4 through 0 in the Command register and bit 2 in the Status Register. The Control Register is unchanged by a programmed Reset. It should be noted that the programmed Reset is slightly different from the hardware Reset (RES); refer to the register description.

sta statusreg: clear overrun
lda I/o reg : e Basta ~~clear~~ I.R. Full -
(+ clear Framing & Parity?)

2